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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Tyler J. Gomm, Frank Alejano and Howard C. Kirsch	Attorney Docket No.:	501035.02
Patent No.	: US 6,803,826 B2	Serial No.	: 10/763,038
Issue Date	: October 12, 2004	Filed	: January 21, 2004
Title	: DELAY-LOCKED LOOP CIRCUIT AND METHOD USING A RING OSCILLATOR AND COUNTER-BASED DELAY		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent in order to correct Patent and Trademark Office errors made during the printing of the patent. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Item (56), Jang Reference	"Jang, Seong-Jin et al., A Compact Ring Delay Line for High Speed Synchronous DRAM, IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1998, pp. 60-61."	--Jang, Seong-Jin et al., "A Compact Ring Delay Line for High Speed Synchronous DRAM," IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1998, pp. 60-61.--

Item (56) Takai Reference	"Takai, Yasuhiro et al., A 250Mb/s/pin 1 Gb Double Data Rate SDRAM with a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme, 1999."	--Takai, Yasuhiro et al., "A 250Mb/s/pin 1 Gb Double Data Rate SDRAM with a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme," 1999.--
Item (57), Line 10	"in put clock signal"	--input clock signal--
Column 3, Line 18	"at a time TO,"	--at a time T**0**,--
Column 3, Line 19	"variable delay VD as a "	--variable delay VD has a--
Column 3, Line 62	"each cycle of the CLK"	--in each cycle of the CLK--
Column 5, Line 15	"present invention a delay-"	--present invention, a delay- --
Column 5, Line 39	"and also coupled"	--and is also coupled--
Column 5, Line 65	"a delayed clock signal."	--of a delayed clock signal.--
Column 5, Line 66	"FIG. **6** a functional"	--FIG. **6** is a functional--
Column 6, Line 37	"receives CLKBUF signal"	--receives the CLKBUF signal--
Column 8, Line 17	"edge is all the CLKBUF"	--edges of the CLKBUF--
Column 8, Line 60	"having a rising-edges"	--having rising-edges--
Column 9, Line 5	"substrate in which the"	--substrate in the--
Column 9, Line 21	"of the clkosc signal"	--of the CLKOSC signal--
Column 9, Line 31	"**606** the operating"	--**606** operating in--
Column 9, Line 33	"having been with rising"	--having rising--
Column 9, Line 40	"detail."	--in detail.--
Column 11, Line 44	"two 32 bits words"	--two 32-bit words--
Column 11, Line 53	"received N/2 bits words"	--received N/2 bit words--
Column 14, Line 7	"being resetresponsive"	--being reset responsive--
Column 14, Line 65	"clock signal an develop"	--clock signal and develop--

The above errors for which correction is requested under 35 U.S.C. § 254 were made in the printing of the patent or in the original application. The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: June 27, 2006 By: Edward W. Bulchis

Edward W. Bulchis, Reg. No. 26,847
Customer No. 27,076
Dorsey & Whitney LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
(206) 903-8785
Attorney for Applicant(s)

EWB:tdp

Enclosures:
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I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 28, 2006 — Date

Alexandra Beggs — Alexandra Beggs

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